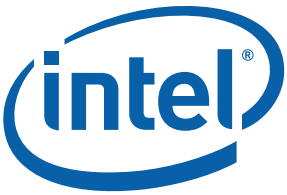


Intel® 41110 Serial to Parallel PCI Bridge

Specification Update

Septembert 2007

Notice: The Intel® 41110 Serial to Parallel PCI Bridge may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 311638-002US

Contents

Revision History

Date	Version	Description
September 2007	002	Added Specification Clarifications 2 and 3. Added Document Change 2.
February 2006	001	Initial release.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual	310183
Intel® 41110 Serial to Parallel PCI Bridge Design Guide	310335
Intel® 41110 Serial to Parallel PCI Bridge Datasheet	310182

Nomenclature

Errata are design defects or errors. These may cause the Intel® 41110 behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 41110 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Plan Fix:	This erratum may be fixed in a future stepping of the product.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings				Page	Status	Errata
	C1	#	#	#			
1	X				10	No Fix	Secondary bus PxPCIRST# pulse prior to the rising edge of PERST#
2	X				10	No Fix	Unable to train in ×1 on Lane 3, 4, or 7 when Lane 0 is broken
3	X				10	No Fix	IOxAPIC End-Of-Interrupt (EOI) register is read/write but should be write-only
4	X				11	No Fix	Unreliable PCI Express link operation when L0s active state power management is enabled
5	X				11	No Fix	Slow edge rates are observed when the Intel® 41110 Serial to Parallel PCI Bridge is driving the PCI-X bus at specific temperatures
6	X				11	No Fix	SSE bit set for PERR# assertion when error reporting is masked
7	X				12	No Fix	Data Parity Error detected on PCI/X interface fails to propagate bad parity
8	X				12	No Fix	Bridge Fails to train down in the presence of a degraded lane
9	X				13	No Fix	PCI Express and PCI-X Header Logs and First Error Pointers do not remain sticky through reset.
10	X				13	No Fix	Incorrect Default Value for PCI Express Flow Control Protocol Error Severity Bit.
11	X				13	No Fix	Power State Bits in PCI Express Power Management Control/Status Register mistakenly accept reserved values.
12	X				14	No Fix	Performance across an Upstream x1 PCI Express Link is less than expected.
13	X				14	No Fix	SKP Ordered Set may not be sent within required interval during link recovery if a packet is pending
14	X				15	No Fix	PCI Express ESD enhancement requires a change to register settings
15	X				15	No Fix	SERR fatal/non-fatal error message enabled with incorrect error message enabled bit
16	X				16	No Fix	Byte Enables (BE) not included in PCI delayed reads can cause data corruption
17	X				16	No Fix	Bridge may become unresponsive when transitioning into the D3 power state.
18	X				17	No Fix	Under certain conditions, inbound prefetched PCI read requests may return wrong data to the requestor
19	X				17	No Fix	Bridge Incorrectly Reports Itself as a Multi-Function Device

Specification Changes

No.	Steppings				Page	Specification Changes
	A1	B0	C0	C1		
1	X	X	X	X	18	L0s state is not supported
2	X	X	X	X	18	Linear Voltage Regulators are Recommended for 1.5 V supplies
3	X	X	X	X	18	Updated Power Sequencing Steps for VCC15 and VCC33 Voltages
4	X	X	X	X	19	Use Microcontroller When Implementing Some Erratum Workarounds
5	X	X	X	X	19	BCNF Bit 3 Changed to Reserved bit
6	X	X	X	X	19	REFCLK relationship to voltage rails

Specification Clarifications

No.	Steppings				Page	Specification Clarifications
	A1	B0	C0	C1		
1	X	X	X	X	20	SMBus connection recommendations for PCI Express* adapter cards
2	X	X	X	X	20	Bridge Device ID corrected to 032D
3	X	X	X	X	21	41x10 interaction with 5V PIC microcontroller may be intermittent

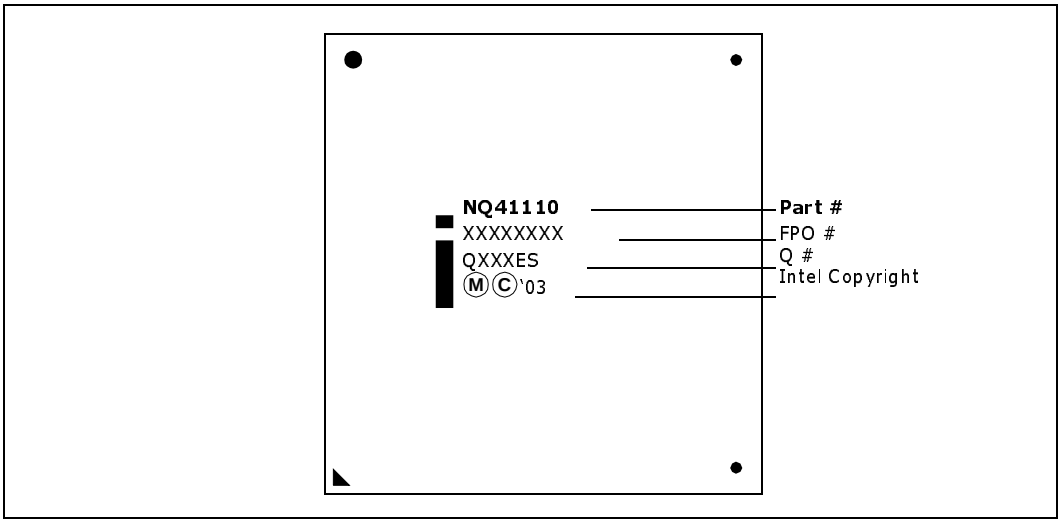
Documentation Changes

No.	Document Revision	Page	Documentation Changes
1	310182 310183 310335	22	L0s state is not supported.
2	310183	22	Device REVID 00h (is an error) and needs to be changed to 09h per the C1 revision

Identification Information

Markings

Figure 1. Marking Information



Part Number	Stepping	Q Number	MM Number[a]	Notes
NQ41110	Production	SL93T	878375	Pb (Leaded)
QG41110	Production	SL93U	878377	Pb free (Lead free)

a. MM = Material Master ID. Reference the MM Number when placing an order.

Errata

1. Secondary bus PxPCIRST# pulse prior to the rising edge of PERST#

Problem: During system power on and prior to the 41110 Bridge receiving the rising edge of PERST#, a pulse is observed on the secondary bus PxPCIRST# signals.

Implication: PCI/PCI-X controllers on the secondary bus segments could interpret this PxPCIRST# pulse as a true rising edge and initialize into an undetermined state.

Workaround: A temporary HW workaround has been identified. The PERST# signal that is received by the 41110 Bridge component should be used to gate the secondary bus PxPCIRST# signals.

Status: No Fix. See the "Summary Table of Changes" on page 6.

2. Unable to train in ×1 on Lane 3, 4, or 7 when Lane 0 is broken

Problem: The 41110 fails to train as a ×1 width on either Lane 3, 4, or 7 when Lane 0 is broken (in other words, not electrically visible to the MCH/XMB/TMB).

Implication: This problem prevents 41110 Bridge training as a ×1 in Lane 3, 4, or 7 (when Lane 0 is broken or otherwise electrically disconnected).

Workaround: None

Status: No Fix. See the "Summary Table of Changes" on page 6.

3. IOxAPIC End-Of-Interrupt (EOI) register is read/write but should be write-only

Problem: The IOxAPIC End-Of-Interrupt register (EOI) (Bus 0, Device 0, Functions 1 and 3, Direct Memory Space Register, Offset 40h) should be write-only. The APIC specification specifies that this register must be implemented as write-only. In the 41110, this register is inadvertently implemented as read-write.

Implication: When implemented as write-only, this register returns the value FFh when read. Since this register is implemented as read-write, the 41110 Bridge returns the "real" value of the register contents when read.

There is no impact to functionality.

Workaround: None.

Status: No Fix. See the "Summary Table of Changes" on page 6.

4. Unreliable PCI Express link operation when L0s active state power management is enabled

Problem: PCI Express* link operation is unreliable after the L0s state is enabled in the 41110 Bridge.

Implication: When L0s is enabled, the system may hang or behave in an unstable manner.

Workaround: The link control register must be written to prevent the 41110 from entering L0s. A platform- dependent BIOS workaround has been identified. Please refer to Specification Changes "L0s state is not supported" on page 18 and to the Intel® 41110 *Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on how to disable L0s support and implement this workaround.

Note: The Intel® 41110 Serial to Parallel PCI Bridge Initialization Customer Reference Code associated to this workaround is available from Intel. Contact your Intel Representative for more information.

Status: No Fix. See the "Summary Table of Changes" on page 6.

5. Slow edge rates are observed when the Intel® 41110 Serial to Parallel PCI Bridge is driving the PCI-X bus at specific temperatures

Problem: Signal-integrity issues may occur at a specific temperature when 41110 Bridge is driving the PCI/PCI-X bus. This issue is highly sensitive to temperature and occurs within a narrow range (1–2 °C) within the normal operating temperature range. The failing temperature varies for each die. The cause of the problem is that a hidden register is loaded with an inappropriate value, causing incorrect drive strength on PCI signals.

Implication: Parity errors and system hangs may occur.

Workaround: Write 1s to the bridge configuration space (address offset 224h, bits[29:17], function 0 and 2). This must be done before any PCI-X bus access occurs. Please refer to the Intel® 41110 *Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on implementing this workaround.

Note: The Intel® 41110 Serial to Parallel PCI Bridge Initialization Customer Reference Code associated to this workaround is available from Intel. Contact your Intel Representative for more information.

Status: No Fix. The workaround must be in place for all steppings of the 41110 Bridge. See the "Summary Table of Changes" on page 6.

6. SSE bit set for PERR# assertion when error reporting is masked

Problem: During a downstream memory write to 41110 Bridge, the following erroneous behavior is seen when PERR# is asserted on the secondary bus:

- Signaled System Error (SSE) in the STS_REG register (D:0, F:0&2, offset 06h, bit 14) is set when SERR# Enable (SEE) (D:0, F:0&2, offset 04h, bit 8) and Parity Error Response Enable (PERE) (D:0, F:0&2, offset 04h, bit 6) are set in the CMD register.
- The PERE bit in the BRDG_CNTL register is set (D:0, F:0&2, offset 3Eh, bit 0).
- Error reporting is disabled in the UNC_PXERRMSK register (D:0, F:0&2, offset 130h).

Implication: False indication of an error message escalated as recorded in SSE of the STS_REG register being set. This is considered low risk since the escalation of the message is functioning properly.

Workaround: None at this time.

Status: No Fix. See the "Summary Table of Changes" on page 6

7. Data Parity Error detected on PCI/X interface fails to propagate bad parity

Problem: In PCI and PCI-X mode using 32-bit data transfers, when a read request gets disconnected at an even dword boundary with data parity error, such that the subsequent request for partial data gets retried, the completion for this request is issued over PCI Express to the MCH (root complex) without the poisoned data EP field set in the PCI-Express TLP header.

Implication: Corrupted Data forwarded without error indication if error escalation is not enabled.

Workaround: Uncorrectable error escalation must be enabled in the MCH and 41110 Bridge to contain this data parity escape. Therefore, a complete workaround for this Erratum will also require MCH/root complex escalate parity errors correctly appropriate platform. Please refer to the Intel® 41110 *Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on implementing this workaround.

Note: The Intel® 41110 Serial to Parallel PCI Bridge Initialization Customer Reference Code associated to this workaround is available from Intel. Contact your Intel Representative for more information.

Status: No Fix. See the "Summary Table of Changes" on page 6

8. Bridge Fails to train down in the presence of a degraded lane

Problem: Problem: During the PCI Express training sequence, if a broken endpoint has correct receiver termination on a lane and transmits training sequences on the lane which are invalid, the 41110 Bridge will fail to link train.

Implication: The PCI Express specification intends that, if some lanes are transmitting bogus data instead of valid training sequences, those lanes should be treated as broken, and the link should fail down to an acceptable width, such as x1. If Lane 0 were failing in this manner, the PCI-E specification would anticipate that the link would fail to train. If a higher-numbered lane were failing in this manner, the PCI-E specification requires that the link attempt to train as a x1 on lane 0. In either case, 41110 Bridge will not train for the problem scenario.

On production material, failures are anticipated to be either a broken transmitter path or a broken receiver path, or a silent transmitter. 41110 Bridge will train properly for these failure modes, since either the receiver termination will be missing, or the transmitted signals will not be seen at the 41110 Bridge. In order to see invalid transmitted data on lanes at the 41110 Bridge, either a logic bug in the other PCI-E endpoint would be required, or a signal integrity issue so severe as to make operation impossible, such as a broken or intermittent connection.

Workaround: None. A non-compliant or broken device could exhibit this erratum.

Status: No Fix. See the "Summary Table of Changes" on page 6

9. PCI Express and PCI-X Header Logs and First Error Pointers do not remain sticky through reset.

The PCI Express and PCI-X header logs and First Error pointers are not maintaining their values after a warm/hot reset. These registers should be unaffected by a warm/hot reset, but instead, they are reset to default values. The following registers with "sticky" bits are affected: ADVERR_CTL (offset 118h), HDR_LOG (offset 11Ch), PCIXERRUNC_PTR (offset 138h), PCIXHDR_LOG (offset 13Ch).

Implication: Errors detected will be logged and escalated properly, but after a warm/hot reset, the header logs and first error pointers will reset to their default values.

Note: Error status registers are unaffected, and properly maintain their values through reset.

Workaround: None at this time.

Status: No Fix. See the "Summary Table of Changes" on page 6

10. Incorrect Default Value for PCI Express Flow Control Protocol Error Severity Bit.

Problem: The PCI Express Flow Control Error Severity bit, register offset 10C, bit 13, is programmed to a default value of 0, indicating an uncorrectable flow control error will be reported as non-fatal. This is in contradiction with the PCI Express Specification, which requires a default value of 1, indicating an uncorrectable flow control error will be reported as fatal.

Implication: Implications for this erratum depend upon the error response strategy implemented in a specific system.

This bit can be reprogrammed to match the specified default value if desired. Refer to the Intel® 41110 *Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on this workaround.

Note: The Intel® 41110 Serial to Parallel PCI Bridge Initialization Customer Reference Code associated to this workaround is available from Intel. Contact your Intel Representative for more information.

Status: No Fix. See the "Summary Table of Changes" on page 6.

11. Power State Bits in PCI Express Power Management Control/Status Register mistakenly accept reserved values.

Problem: The Power State bits, bit 1:0 of PM_PMCSR (Offset 70h) will allow a reserved value of 01 or 10 to be written. This is contrary to the specification, which originally stated that if software attempted to write an unsupported reserved state to this field, the data would be discarded and no state change would occur.

Implication: If a reserved state is written to this field, there will be a mismatch between the actual power state of the part and the state reported in configuration space. In some cases, writing a reserved value to this field could cause the 41110 Bridge to transition to the D0 power state, regardless of the previous power state.

Workaround: Never write a reserved value to this bit field.

Status: No Fix. See the "Summary Table of Changes" on page 6.

12. Performance across an Upstream x1 PCI Express Link is less than expected.

Problem: When the 41110 Bridge is configured with an upstream x1 PCI Express link, the realized performance is significantly less than the predicted linear assumption that a x1 link will provide ¼ the performance of a x4 link. This is caused by circumstances where 41110 Bridge must discard a large portion of the data it receives across the upstream link. Notably; anytime 41110 Bridge services an incorrect prefetch, or anytime 41110 Bridge services interleaved requests from multi-function devices, 41110 Bridge must discard data.

The problem occurs because, in PCI mode, the target memory has no indication of the amount of data to send in response to a read request. It must rely upon prefetch policy and disconnects. If a disconnect occurs, it must discard (possibly stale) data. Data that is discarded after consuming bandwidth on the PCIe bus must then be re-read and can become a significant percentage of the available PCIe bandwidth.

Single-function masters on a PCI bus segment typically do not exhibit this behavior. Multi-function devices and/or multiple devices on a PCI bus segment are more likely to cause this problem, since they are likely to interleave read requests, which is a primary cause of data discard.

This problem has not been seen in PCI-X, because byte counts of read requests are known, buffers are preallocated and data does not need to be discarded.

Implication: Devices that rely heavily on prefetching, or multi-function devices that request data in an interleaved fashion are the most likely to experience degraded performance.

Workaround: System designers should reduce the amount of prefetching allowed to devices behind 41110 Bridge if possible.

Status: No Fix. See the "Summary Table of Changes" on page 6

13. SKP Ordered Set may not be sent within required interval during link recovery if a packet is pending

Problem: During Link Recovery on the PCI Express port, the device may fail to transmit a SKP Ordered set within the required time interval as defined in the PCI Express 1.0a Specification if a TLP or DLLP was pending when the link entered Recovery.Idle state.

Implication: If the receiving device depends upon receipt of a SKP Ordered set to progress through Link Recovery, a timeout will occur resulting in Link Down and automatic reinitialization of the PCI Express Link. A link transitions through Recovery only under exceptional operational conditions. Following the Link Recovery timeout and reinitialization, the PCI Express link should resume normal operation unless the original Link Recovery condition was entered as a result of a hard failure mechanism.

Workaround: None.

Status: No Fix. See the "Summary Table of Changes" on page 6.

14. PCI Express ESD enhancement requires a change to register settings

Problem: Validation has shown PCI Express ESD enhancement, with changes to undisclosed registers in the 41110 Bridge.

Implication: The workaround that follows increases the margin for the eye and results in a healthier, improved PCI Express link.

Workaround: Set F0/F2:R260h bit[15] to 1 and clear F0/F2:R270h bit[31] to 0. This workaround is required for both cold and warm reset. Refer to the *Intel® 41110 Serial to Parallel PCI Bridge Initialization by the SMBus using the PIC16F876A Microcontroller White Paper* (302281) for details on implementing this workaround.

Note: The Intel® 41110 Serial to Parallel PCI Bridge Initialization Customer Reference Code associated to this workaround is available from Intel. Contact your Intel Representative for more information.

Status: No Fix. See the "Summary Table of Changes" on page 6.

15. SERR fatal/non-fatal error message enabled with incorrect error message enabled bit

Problem: When Secondary bus SERR errors are not being escalated (i.e., when the SERR# Enable (SEE) bit in the PCI Command Register (offset 0x4) is not set), then the Advanced Error Reporting scheme concerning SERR configuration is flawed. Specifically, when SERR is configured as a fatal error, the generation of a SERR fatal error message is mistakenly gated by the Non-Fatal Error Reporting Enabled bit (bit[1]) instead of the Fatal Error Reporting enabled bit (bit[2]) of the Device Control Register (offset 4Ch). Likewise, when SERR is configured as a non-fatal error, the generation of a SERR non-fatal error message is gated by the Fatal Error Reporting enabled bit.

Implication: The SERR fatal error message can be generated only when non-fatal error messaging is enabled, and the SERR non-fatal error message can be generated only when fatal error messaging is enabled.

Workaround: The workaround for this errata is implementation specific. The following are options for working around this errata:

- ..... Set the SERR# enable bit in PCI command register (offset 0x4 - bit 8)
- ..... For Advanced Error reporting:
  Set the Report NonFatal and Fatal Error bits (offset 0x4C - bits 1 and 2).
- ..... If using the Advanced Error reporting capability for SERR# escalation as Fatal (ERR_FATAL):
  Set the Report NonFatal Error enable bit (offset 4c, bit 1) and mask other PCI-X errors that are set to NonFatal, using offset 0x134 and 0x130, if escalation of those errors is not desired.
- If using the Advanced Error reporting capability for SERR# escalation as Non-Fatal (ERR_NonFATAL):
  Set the Report Fatal errors enable bit (offset 4c, bit 2).

Status: No Fix. See the "Summary Table of Changes" on page 6.

16. Byte Enables (BE) not included in PCI delayed reads can cause data corruption

Problem: A PCI device on one of the secondary busses that generates a zero length read request may cause data corruption in platforms utilizing non-Intel MCH components, as the byte enables (BE) are not included by the 41110 bridge in matching completions to PCI delayed read requests.

Implication: All Intel MCH devices will return data consistent with the address of a zero-length read request. No corruption can occur if a subsequent non-zero-length read is inadvertently completed with data returned on behalf of the zero-length request but this behavior is not required by specification.

The following is an example case:

1. A memory read request with zero BE is issued over PCI, a corresponding zero length read results on PCI-Express to the host.
2. A PCI device on the same PCI segment issues a MR/MRL/MRM to the same address with valid BE's.
3. The 41110 bridge matches the completion for the Memory Read request on line 1 to the request on line 2 (i.e. - BE's are ignored.)
4. Unspecified data (returned for the zero-length read request) is driven to the PCI card, resulting in data corruption.

Note: This exclusively affects PCI mode and is not an issue when the secondary busses are operating in PCI-X mode. Whether corruption can occur through this mechanism is dependent upon behavior of the non-Intel MCH component. If the MCH in use behaves similarly to Intel MCH designs, there is no exposure to data corruption, and the incomplete completion match will not have any side-effects.

Workaround: None.

Status: No Fix. See the "Summary Table of Changes" on page 6.

17. Bridge may become unresponsive when transitioning into the D3 power state.

Problem: When the 41110 Bridge transitions to a power state of D3 or lower, the 41110 Bridge may become unresponsive.

Implication: There have been no observed failures on systems with currently available software. Operating systems that independently manage the power state of the 41110, outside the scope of system level power state transitions, may result in the loss of link communications to the MCH.

Workaround: Independent device power state management of the 41110 should be avoided. If the 41110 Bridge becomes unresponsive, a fundamental device reset must be asserted to return the system to normal operation.

Status: No Fix. See the "Summary Table of Changes" on page 6.

18. Under certain conditions, inbound prefetched PCI read requests may return wrong data to the requestor

Problem: With some prefetch policy settings, the 41110 may over-aggressively prefetch data for PCI reads and subsequently return the wrong data to the requestor. This problem only exists when there is more than one active agent on the PCI bus. It exists for all supported frequencies and exists on both 41110 PCI segments. It does not effect PCI-X operation at any supported frequency.

Implication: Inbound read requests that are enabled for prefetching may return invalid data when multiple agents exist on the same PCI bus. No error is reported by the 41110.

Workaround: Set D0:F0/F2 Offset 184h (Dword) bit [2] to 1. The workaround corrects the problem at all supported frequencies and all prefetch policy settings.

Status: No Fix. Not to be fixed. The workaround must be left in place for all 41110 steppings. See the "Summary Table of Changes" on page 6.

19. Bridge Incorrectly Reports Itself as a Multi-Function Device

Problem: The multi-function bit is set ON in the Header Type configuration register, offset Eh, identifying that there are multiple functions associated with the device when there is only one.

Implication: Configuration software assumes that there are multiple devices behind the bridge and may perform unnecessary operations.

Workaround: None. Software needs to verify that a function is valid before taking action.

Status: No Fix. Not to be fixed. See the "Summary Table of Changes" on page 6.

Specification Changes

1. L0s state is not supported

Issue: The L0s state has been defeatured in the 41110 Bridge.

Affected Docs: Intel® 41110 Serial to Parallel PCI Bridge Datasheet (278885-001)
Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual (278890-001)
Intel® 41110 Serial to Parallel PCI Bridge Design Guide (278801-001)

2. Linear Voltage Regulators are Recommended for 1.5 V supplies

Issue: Linear Voltage regulators are recommended when using 1.5 Volt power supplies.

Affected Docs: Intel® 41110 Serial to Parallel PCI Bridge Design Guide (278801-001)

3. Updated Power Sequencing Steps for VCC15 and VCC33 Voltages

Issue: The following three steps are the power sequencing requirements that must be followed with the 41110 Bridge:

1. The 41110 Bridge requires that the VCC33 voltage rail be no less than 0.5V below VCC15 (absolute voltage value) at all times during 41110 operation, including during system power up and power down. In other words, the following must always be true:

   VCC33 >= (VCC15 – 0.5V)

   This can be accomplished by placing a diode (with a voltage drop <0.5V) between VCC15 and VCC33. A node will be connected to VCC15 and cathode will be connected to VCC33.

   If VCC15 (1.5V PCI-X I/O voltage) and VCC (1.5V core voltage) are tied together on the platform, then both voltages must meet the above rule.

Note: Linear voltage regulators are recommended when using 1.5 Volt power supplies.

2. If a voltage regulator solution is used which shunts VCC15 to ground while VCC33 is powered, the maximum allowable time that VCC15 can be shunted to ground while VCC33 is fully powered is 20ms. This includes configurations where VCC and VCC15 are powered by the same power source.
3. The maximum allowed time between VCC33 and VCC15 ramping is 525ms.

Note: There is no minimum sequencing time requirement other than requirements in Steps 2 and 3.

Affected Docs: Intel® 41110 Serial to Parallel PCI Bridge Design Guide (278801-001)

4. Use Microcontroller When Implementing Some Erratum Workarounds

Issue: The workarounds for a number of erratum observed in the 41110 Serial to Parallel PCI Bridge (Erratum 19, 20, 25, 28, and 32) require that Configuration Space registers be loaded with specific values. Intel requires that this be done using the microcontroller attached to the 41110 Bridge SM Bus prior to releasing the CFGRETRY signal.

Affected Docs: Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual (278890-001)
Intel® 41110 Serial to Parallel PCI Bridge Design Guide (278801-001)

5. BCNF Bit 3 Changed to Reserved bit

Issue: Bit 3 in the Bridge Configuration Register (Offset 40 in both A- and B- bridges) is currently defined as 'Downstream Delayed Transaction Resource Partitioning (ODTP)' with a default setting of '0'. Setting this bit to '1' may cause undesired functionality; therefore BCNF.3 is changed to 'reserved'. As a 'reserved' bit, the default condition of '0' should be maintained and BIOS firmware should never set this bit to a '1'.

Affected Docs: Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual (278890-001).

6. REFCLK relationship to voltage rails

Issue: When the 41110 is on an add-in card, only 3.3V and 12V are provided to the slot, therefore, a local regulator is required for 1.5V and 2.5V generation. Due to the delay by the local regulators, REFCLK may already be provided before the power rails are stable. If this is the case, no device overstress will occur, provided that the REFCLK input current does not exceed 900mA and the input voltage does not exceed the PCI Express specification of 1.15V. REFCLK buffers on many Intel platforms show an input current of 15.6mA, well under the 900mA limit.

The requirement for "all 41110 voltage rails to be stable before the PCI Express differential clocks REFCLKp and REFCLKn begin running" is no longer a requirement.

Affected Docs: Intel® 41110 Serial to Parallel Bridge Design Guide (278801-003)

Specification Clarifications

1. SMBus connection recommendations for PCI Express* adapter cards

Issue: PCI Express* cards based on the 41110 Bridge must implement the SMBus signals in one of the following ways:

1. The SMDAT and SMCLK signals from the PCI Express* connector must be left as "no connects". The SMBCLK and SMBDAT signals on the 41110 must have pull-ups even when they are not used. The pull-ups prevent the inputs from oscillating and potentially causing other problems.
2. When the SMBus feature is required, an isolation device (for example, the LTC4301) must be placed between the SMBus signals on the PCI Express* connector and the 41110, so that the system has no connection to the 41110 on these two signals when power is off.

For embedded/backplane designs, it is assumed that the SMBus is routed only to devices that are required and that remain powered

Affected Docs: *Intel® 41110 Serial to Parallel PCI Bridge Datasheet*
and
Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual

2. Bridge Device ID corrected to 032D

Issue: In section 12.2.1, Table 35, of the 41110 Developer's Manual, bits [31:16] incorrectly state the device ID for the 41110. Bits [31:16], in Section 12.2.1, Table 35, now appears as follows:

12.2.1) Offset 00h: ID—Identifiers¶

Contains the vendor and device identifiers for software.¶

Table 35.) Offset 00h: ID—Identifiers §

Bits§	Type§	Reset§	Description§
31:16§	RO§	032D§	Device ID (DID): These bits indicate the device number assigned by Intel to the Intel® 41210 Serial to Parallel PCI Bridge. §
15:0§	RO§	8086h§	Vendor ID (VID): This 16-bit field indicates that Intel is the vendor.§

Affected Docs: *Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual*.

3. 41x10 interaction with 5V PIC microcontroller may be intermittent

Issue: The Intel 41x10 Customer reference board contains an error that may prevent proper operation on the PIC microcontroller. The 41x10, a 3.3V logic device is asserting a signal to a Schmitt trigger input of a 5V part (PIC Microcontroller - PIC16F876A - requires 4V for a logic high on the Schmitt trigger input). In certain cases, the PIC microcontroller may not detect the logic high and thus fail to execute the PIC initialization code.

Only designs which leveraged the 41x10 reference board with the implemenation of the 5V PIC microcontroller are affected. Implementations using a 3.3V microcontroller are not affected by this issue.

A fix to the PIC initialization reference code has been identified to workaround this issue.

Note: The Intel 41x10 Serial to Parallel PCI Bridge Initialization Customer Reference Code associated with this fix is available from Intel. Contact your Intel representative for more information.

Affected Docs: *Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual*.

Documentation Changes

1. L0s state is not supported.

Issue: The L0s state has been defeatured in the 41110 Bridge.

Affected Docs: *Intel® 41110 Serial to Parallel PCI Bridge Datasheet*
Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual
Intel® 41110 Serial to Parallel PCI Bridge Design Guide

2. Device REVID 00h (is an error) and needs to be changed to 09h per the C1 revision

Issue: Table 38 in the *Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual* indicates that the Offset for REVID - Revision ID is 00h. It should look as indicated below:

New Text: Highlighted in RED.

12.2.4 Offset 08h: REVID—Revision ID

This register is the Revision ID Register.

Table 38. Offset 08h: REVID—Revision ID

Bits	Type	Reset	Description
7:0	RO	09h	**Revision ID (RID):** These bits indicate the stepping (die version) of the Intel® 41110 Serial to Parallel PCI Bridge. 0000 1001 C-1 stepping

Affected Docs: *Intel® 41110 Serial to Parallel PCI Bridge Developer's Manual*.